

## ABSTRACT OF THE DISCLOSURE

There is provided a scan test system comprising: a semiconductor device including a scan register connected  
5 between an input/output pin on an analog input side and an internal system logic; a semiconductor device including a scan register connected between an input/output pin on an analog output side and an analog sensor; and an analog wiring connecting the input/output pins each other. Thus, the scan  
10 register can be chained to thereby constitute a boundary scan register chain, and thereby JTAG control can be carried out by use of TAPC. Therefore, monitoring inspection where probes are set up by means of high-density-assembling of semiconductor devices and the multiple pins of low-cost devices, can be  
15 achieved.

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